THREADX MIPS

ThreadX Highlights

- Complete MIPS Architecture Support, including MIPS32 4Kx, 5Kx, 14Kx, 24Kx, 34Kx, 1004Kx, PIC32MX, PIC32MZ, interAptiv, microAptiv
- Reasonable Pricing
- **No Royalties**
- Complete ANSI C Source Code
- MISRA-C:2004 and MISRA C:2014 Compliant
- Safety-Certification for IEC 61508 SIL 4, IEC 62304 Class C, ISO 26262 ASIL D, UL/IEC 60730, UL/IEC 60335, UL 1998, and EN 50128 SW-SIL 4
- Easy to use API
- Small Size & Scales Automatically
- Fast Real-Time Response
- Picokernel™ Architecture
- Preemption-Threshold™ Technology
- Event-Chaining™ Technology
- Run-Time Stack Analysis
- Run-Time Performance Metrics
- Event-Trace Capability
- Unlimited Threads, Queues, Event Flags, Semaphores, Mutexes, Timers, Block and Byte Memory Pools
- Deterministic Processing
- Optimized Application Timers
- Fully Integrated with FileX, GUIX, NetX, NetX Duo, and USBX
- Extensive Development Tool Choices
  - Green Hills MULTI
  - Microchip MPLABX
  - GNU
- ThreadX Kernel Aware Debugging
  - Green Hills MULTI
  - Imagination Codescape
  - Microchip MPLABX
  - Lauterbach
- Optimized Interrupt Handling
  - Only compiler scratch registers saved at the beginning of ISR
  - Most ThreadX services are allowed from ISRs
  - System stack used in ISRs
  - Nested Interrupt Support

Small Footprint (all sizes in bytes)

Instruction Area Sizes	
Core Services:	**3,532**
Queue Services:	924
Event Flag Services:	764
Semaphore Services	376
Mutex Services:	1,208
Block Memory Services:	440
Byte Memory Services:	912

RAM Sizes	
Global Data Area:	1-2KB
Thread Control Block	188
Timer Control Block:	44
Queue Control Block:	60
Semaphore Control Block:	32
Mutex Control Block:	52
Event Flag Control Block:	40
Block Memory Control Block:	48
Byte Memory Control Block:	52

Fast Execution (PIC32MX Processor @80MHz)

	IR	TS	TR	TRCS
tx_thread_suspend	0.8µs	1.9µs	-	-
tx_thread_resume	-	-	0.8µs	2.3µs
tx_thread_relinquish	0.4µs	-	-	1.9µs
tx_queue_send	0.8µs	2.2µs	1.6µs	3.1µs
tx_queue_receive	0.8µs	2.2µs	2.2µs	3.6µs
tx_semaphore_get	0.4µs	2.0µs	-	-
tx_semaphore_put	0.4µs	-	1.4µs	2.8µs
tx_mutex_get	0.7µs	2.2µs	-	-
tx_mutex_put	0.9µs	-	2.1µs	3.5µs
tx_event_flags_set	0.6µs	-	1.6µs	3.0µs
tx_event_flags_get	0.7µs	2.3µs	-	-
tx_block_allocate	0.6µs	2.2µs	-	-
tx_block_release	0.5µs	-	1.4µs	2.9µs
tx_byte_allocate	1.8µs	2.8µs	-	-
tx_byte_release	1.1µs	-	3.4µs	4.3µs

Context Switch (CS):	1.5µs
Boot Time (BT):	8.0µs
Interrupt Latency Range (ILR):	0.0µs - 0.8µs

Immediate Response (IR): Time required to process the request immediately, i.e., no thread suspension or thread resumption.
Thread Suspend (TS): Time required to process the request when the calling thread is suspended due to unavailability of the resource.
Thread Resumed (TR): Time required to process the request when a previously suspended thread (of the same or lower priority) is resumed as a result of the request.
Thread Resumed and Context Switched (TRCS): Time required to process the request when a previously suspended higher-priority thread is resumed as a result of the request. Since the resumed thread is higher-priority, a context switch to the resumed thread is also performed from within the request.
Context Switch (CS): Time required to save current thread's context, find highest priority ready thread, and restore its context.
Boot Time (BT): Time required from tx_kernel_enter to the dispatch of the first thread.
Interrupt Latency Range (ILR): Amount of time interrupts are disabled.

expresslogic 11423 West Bernardo Court, San Diego, CA 92127 • 1-858-613-6640 tel • 1-858-613-6646 fax