SoCe

System-on-Chip *engineering*

FPGA based Solutions

for Communications in Critical Systems

2016

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SOCe

Company Profile

Located in Bilbao (Spain), SoC-e is one of the worldwide leading suppliers of Ethernet communication solutions based on FPGA technology. SoC-e is pioneer developing a portfolio of IP cores that implement the leading-edge networking and synchronization technologies for critical systems.

It was founded in 2010 by a group of senior engineers and researchers from the University of the Basque Country (UPV/EHU) with a very strong expertise in embedded systems, networking and reconfigurable technology.

SoC-e has invested a large effort on R&D activity to develop optimized hardware and software architectures to face the challenges that have arisen when implementing these standards. In the same way, SoC-e takes part in most of the interoperability events contributing to the testing and spreading of these new technologies. In order to allow this intensive R&D activity and in internationalization, this company has reinvested all the profits since its creation and it has enforced its strategy with the integration of SoC-e in Etxe-Tar Corporation, an industrial group reference in innovation.

SoC-e has extended the offer of these added-value technologies, developing families of FPGA and SoC based pluggable modules. This solution reduces the time-to-market and the development risk of the final product for the customer.

Nowadays, SoC-e technology is present in more than 20 countries worldwide. Our customers are multinationals and SMEs of the Electric, Industrial and Aerospace sectors that select SoC-e IPs, modules and end-equipment for their products and projects.

SoC-e evolves for your advantage. The powerful technologies developed have to be combined to offer the customer the optimal solution for the proposed requirements. Therefore, it is SoC-e mission giving to each project and to each customer personalized support. The SoC-e Team grows continuously with additional MsC and PhD professionals in fields like middleware software, multi-processor computing and cybersecurity to ensure that we provide to our customers with the best added-value solutions.

SoC-e evolution is also focused on enforcing its partnership activity. The network of agents and distributors includes partnerships in South Korea, USA, Germany and Israel. Nowadays, SoC-e is Xilinx Alliance Certificate Member and Xilinx´s reference partner for Smart-Grid solutions.

We hope that the present catalogue works as a high level overview of what SoC-e can offer to your technology roadmap. The challenges of Industrial IoT and Cybersecurity invite us to be pionners once again and we will be glad to share this vision with you.

Technology

How HSR Provides Network Redundancy

High-availability Seamless Redundancy (HSR, IEC 62439-3-Clause 5) provides redundancy by sending packets in both directions through a ring network.

A simple HSR network consists of Doubly Attached Bridging Nodes, each having two Ethernet ports. A HSR node sends the same frame over both ports.

A HSR capable destination node receives, in fault-free state, two identical frames over both ports respectively within a certain interval. The first received frame is accepted while the duplicate is discarded. In case of an interruption in the ring, the frame will always be received through the other port.

HSR offers "zero-recovery" time in case of failure of one component. Thus, high availability and very short reaction time.

The end-node works as a switch, so the space and cost saving can be meaningful.

How PRP Provides Network Redundancy

Parallel Redundancy Protocol (PRP, IEC 62439-3-Clause 4) redundancy is implemented in the nodes rather than in the network. Especially adapted nodes (Dual Attached Nodes- DANs), are connected to two independent Ethernet networks (LAN A and LAN B), and send the same frames over both networks.

In a fault-free state, destination nodes consume the first received frame and discard the duplicates. In case of a fault in one of the networks, the frames will still be transmitted and received through the other.

Non-PRP nodes can be attached to a single Network, thus they communicate only with nodes attached to this network, or connected to both Networks through a RedBox.

How IEEE 1588 PTP Provides Network Synchronization

IEEE1588 PTP protocol is able to synchronize networked clocks with accuracy down to the nanosecond range. It provides high precision combined with easy installation compared with alternative synchronization mechanisms (NTP, GPS, IRIGb, etc.).

It is based on the Packet Locked Loop (PLL) approach. Like any active synchronized circuit, the IEEE1588 clock is a servo implemented with a closed-loop algorithm of some sort.

It allows systems synchronization and data transfer to use the same standard Network, Ethernet in most cases. It requires minimal network, computing and hardware resources so it can be applied to low-cost as well as to high-end devices.

How TSN Merges Factory and Enterprise Networks

Industrial Internet of Things (IIoT) offers smarter infrastructure and hyper-connected devices with sensing, processing and networking capabilities. These systems will generate incredible amounts of data, sharing the same network. Thus, it is necessary to ensure that the real-time and critical-mission messages are transferred within strict bounds of latency and reliability regardless of other network traffic.

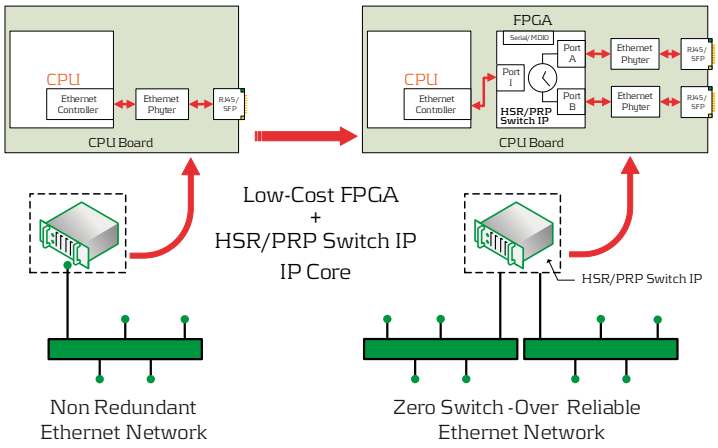
TSN stands for Time Sensitive Networking. It is the name of the IEEE 802.1 Task Group responsible for standards at Data Link Layer. This group provides the specifications that will allow time-synchronized, low latency, streaming services through IEEE 802 networks.

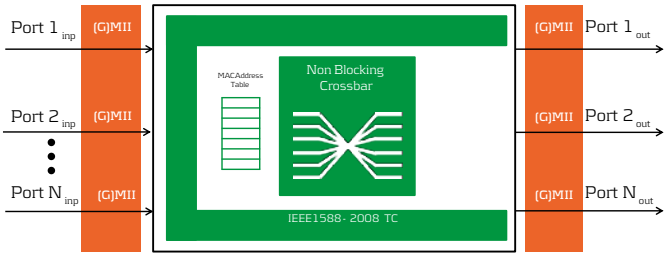
TSN is unique in that its streams are delivered with guaranteed bandwidth and deterministic latency. There are many features involved in the multiple standards currently under development.

TSN is evolving and it is targeting different sectors, like Automotive, Industry, Broadcasting and Aerospace. Therefore, new swithching implementation will arise that combine a subset of the available standards and features. This flexibility can be achieved through reconfigurable logic (FPGAs), HDL IPs and embedded software.

IP Cores for FPGAs

Networking





HSR/PRP Switch IP

This IP implements bumpless Ethernet connectivity ensuring zero-delay recovery time in case of network failure and no-frame lost. The IP supports version 3 of High-availability Seamless Redundancy (HSR) and Parallel Redundancy Protocol (PRP) with redundant IEEE 1588-2008. The flexibility and scalability of this IP offers optimized solutions for cost-sensitive CPU-less equipments and for high-end complex MPSoC based networking platforms.

Key Features

- IEC 62439-3 (clauses 4-5) v3
- Up-to 12 ports
- 10/100/1000BaseT-X
- IEEE1588-2008 support
- Cut-through and Store&Forward
- Supervision frames and IEEE 1588-2008 processed by hardware
- CPU-less version available
- Distributed memory architecture for maximum reliability
- Traffic segregation based on Ethernet Type
- 802.1X hardware support
- Reference designs for Spartan-6, 7-Series, Zynq, MPSoC

Ethernet Switch IP Family

- »Managed Ethernet Switch IP
- »Unmanaged Ethernet Switch IP
- »Profinet Switch IP
- »Ethernet IP/DLR Switch IP
- »Media Redundancy Protocol (MRP) Switch IP
- »Cyber-Security Surveillance Switch IP
- »Time Sensitive Networking Switch IP

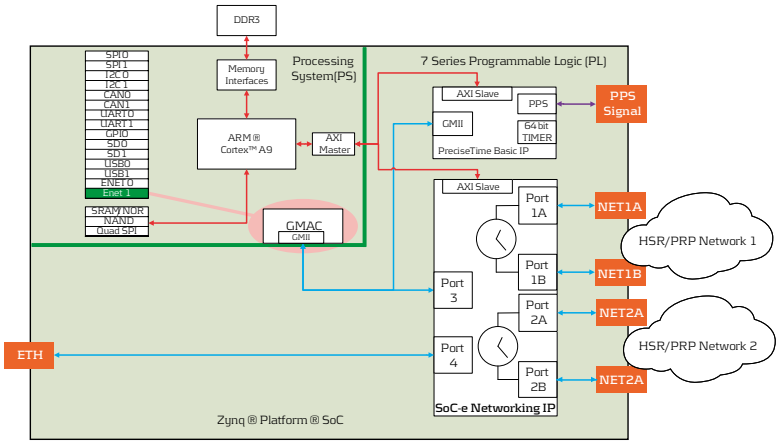
The integration of Ethernet Switches on FPGA is simplifying the communication between heterogeneous systems and applications. Thanks to the flexibility of reconfigurable devices combined with networking IPs, the end-equipment embeds not only Ethernet end-point capabilities but added-value switching features as well. In addition, the low latency of SoC-e IPs implemented over a non-blocking matrix infrastructure is a robust base for networking in critical systems. IEEE 1588-2008 is also supported and even the P2P mode of operation is implemented by hardware. This feature ensures port scalability and simplifies the integration of the IP. SoC-e has developed a portfolio of Ethernet Switching IPs focused on different applications and sectors. Thus, it is feasible combining the features of different IPs to obtain an optimal solution for each case.

General Key Features

- Up-to 12 ports
- 10/100/1000BaseT-X supported
- IEEE 1588-2008 P2P/E2E Transparent Clock operation run by hardware
- Non-blocking matrix architecture: 100% data throughput
- Reference designs for Spartan-6, 7-Series, Zynq, MPSoC

IP Cores for FPGAs

Networking



Managed Ethernet Switch IP

Key Features

- Port based VLAN support
- Switching Portmask
- QoS Priorities (PCP-802.1p, DSCP TOS, Ethertype)
- IEEE 802.1X hardware support
- RSTP hardware support
- Configuration link options: MDIO, UART, AXI4, Configuration-over-Ethernet

Unmanaged Ethernet Switch IP

Key Features

- Plug&Work operation
- Optimized for maximum performance with minimal FPGA resources

Profinet Switch IP

Key Features

- Profinet RT CC-B Line Structure supported
- Multiport support
- Zynq Reference Design available with PORT.DE Profinet software stack

Ethernet IP/DLR Switch IP

Key Features

- Multiport support
- DLR management supported by hardware by port pairs
- Beacon processed by hardware (transmission and reception)

Media Redundancy Protocol (MRP) Switch IP

Key Features:

- MRP hardware processing (no software required)
- Media Ring Manager (MRM) supported
- Media Ring Client (MRC) supported

Cyber-Security Surveillance Switch IP

Key Features:

- Port mirroring for selected ports
- Traffic classification attending traffic type (different queues)
- Zynq reference design under Linux (SMARTzynq board)
- Non-intrusive hardware support for Network Intrusion Detection Systems (NIDS)

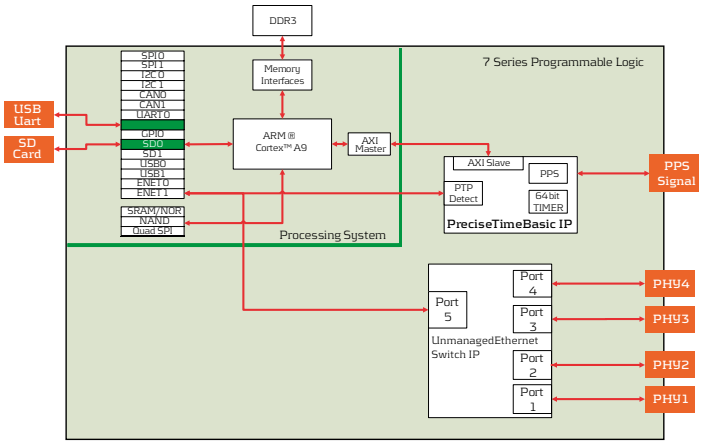
Time Sensitive Networking Switch IP

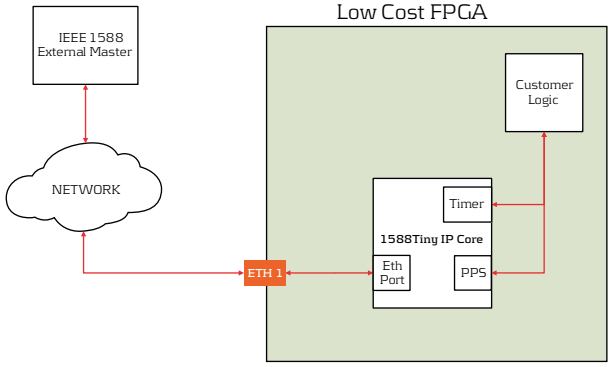
Key features:

- IEEE 802.AS (IEEE 1588-2008 v2 P2P - Layer 2, 802AS profile)
- Standard in draft, technical development in process:
  - » Redundancy: P802.1CB
  - » Frame preemption: P802.1Qbu
  - » Schedule traffic: P802.1Qbv
  - » Traffic policer to limit the excess traffic
  - » Traffic shaper to limit the transmit rate

IP Cores for FPGAs

Synchronization





IEEE 1588-2008 Precise Time Basic IP

The integration of this IP in your design provides an outstanding synchronization mechanism that only requires Ethernet connection to obtain nanosecond range synchronized timers in your equipment. This IP is capable of accurately timestamp IEEE 1588 telegrams and it also embeds the timer. All these processes are carried out by hardware modules.

Key Features

- Hardware and software to support Ordinary , Transparent and Boundary Clock functionalities
- Available for Spartan-6 and 7-Series Xilinx FPGA families
- (G)MII Interfaces supported
- 32 bit seconds / 32 bit nanoseconds counter
- 32 bit sub-nanosecond frequency adjust
- Pulse Per Second (PPS) Output available
- Frequency Selectable Output available (1 KHz/2 KHz/4 KHz/8 KHz/16 KHz/32 KHz)
- IRIG-B Master Output
- PTP on both Layer 2 (Ethernet) and Layer 3 (IPv4) interfaces supported
- Seamless integration with HSR-PRP and Ethernet IP Switch cores
- VLAN support
- IEEE 1588 Profiles supported:
  - » Default
  - » Power
  - » Power-Utility (IEC61850-90-3)
  - » 802.1AS

1588Tiny Slave-Only IP

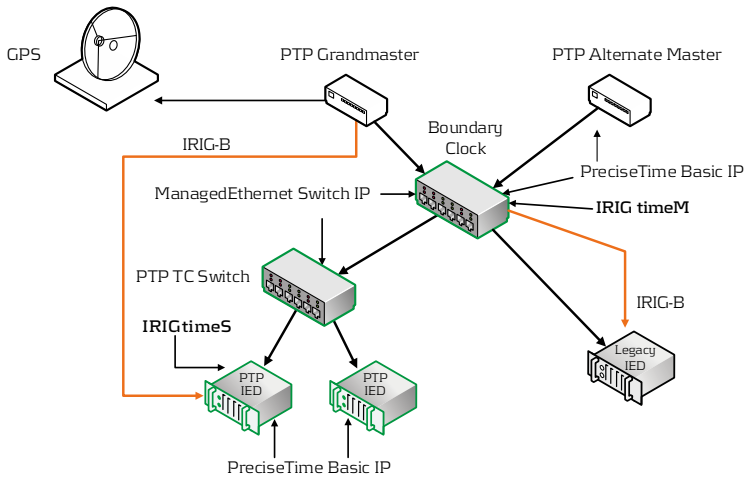
This IP offers the simplest solution available in the market to integrate IEEE 1588-2008 slave capabilities to any equipment. 1588Tiny embeds the Ethernet MAC, the parsing and timestamping units, and the computation logic to output a synchronized clock and a PPS signal. This IEEE1588-2008 V2 hard-only compliant clock synchronization IP core is focused on equipments that require basic IEEE 1588 functionality using the minimum resources and complexity. Therefore, 1588Tiny does not require any software. It can run in CPU-less boards and it can be embedded also with HSR-PRP and Ethernet IP Switch cores that provide hardware supported Transparent Clock operation.

Key Features

- CPU-less operation (no software required)
- IEEE 1588-2008 slave-only operation
- 64 bit Timer value available to customer logic
- (G)MII Interfaces supported
- PPS output signal
- Optional IRIG-B Master Output
- Profiles supported:
  - » Default
  - » Power
  - » Power-Utility (IEC61850-90-3)
  - » 802.1AS

IP Cores for FPGAs

Synchronization



IRIG-B Master IP

This IP implements an IRIG 200-04 compliant time synchronization master on FPGA devices. It has been designed to support all the IRIG-B coded expressions as well as DCLS and AM modulations providing the maximum flexibility and accuracy.

Key Features

- IRIG 200-04 compliant time synchronization master
- Support for DCLS and AM modulations
- Support for all IRIG-B coded expressions, including year information, control functions and straight binary seconds
- Output type (IRIG-B timecode) configurable both before implementation and on-the-fly
- Precise IRIG-B output in order to provide nanosecond precision
- 32-bit timestamp input for initial set up of the IP
- Periodic pulse output for testing
- Autonomous operation by hardware

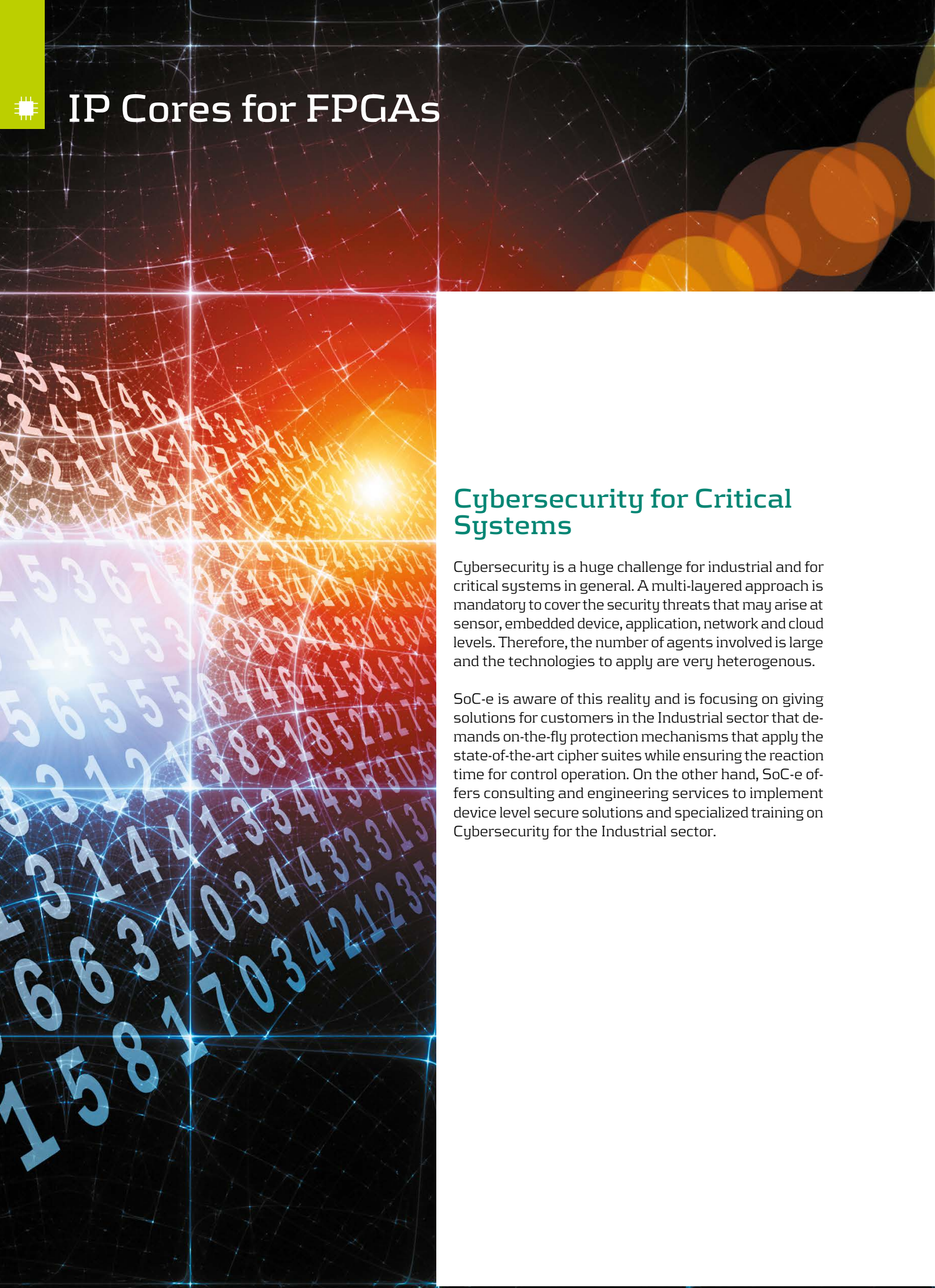
IRIG-B Slave IP

This IP implements an IRIG 200-04 compliant time synchronization slave on FPGA devices. It has been designed to support all the IRIG-B coded expressions as well as DCLS and AM modulations in order to provide maximum flexibility, accuracy and autonomy.

Key Features

- IRIG 200-04 compliant time synchronization slave
- Support for DCLS and AM modulations
- Support for all IRIG-B coded expressions, including year information, control functions and straight binary seconds
- Sub-microsecond synchronization with the IRIG-B master
- 64-bit internal timer synchronized in time and frequency with the IRIG-B master
- 32-bit for timestamp in seconds and 32-bit for nanoseconds
- Periodic pulse output for testing
- Autonomous operation by hardware

IP Cores for FPGAs



Cybersecurity for Critical Systems

Cybersecurity is a huge challenge for industrial and for critical systems in general. A multi-layered approach is mandatory to cover the security threats that may arise at sensor, embedded device, application, network and cloud levels. Therefore, the number of agents involved is large and the technologies to apply are very heterogenous.

SoC-e is aware of this reality and is focusing on giving solutions for customers in the Industrial sector that demands on-the-fly protection mechanisms that apply the state-of-the-art cipher suites while ensuring the reaction time for control operation. On the other hand, SoC-e offers consulting and engineering services to implement device level secure solutions and specialized training on Cybersecurity for the Industrial sector.

IP Cores for FPGAs

Cybersecurity

Substation Automation Systems (SAS) Crypto-core IP

This IP faces the challenge of securing the most time-critical control messages in SAS and Smart-Grid: GOOSE and Sample Measured Values. The new generation of equipment for these specialized sectors needs to offer the highest level of reliability and security. Thanks to this IP, it is feasible implementing the most exigent security standards maintaining the mandatory reaction time defined in the IEC 61850 standard.

Key Feature:

- GOOSE & SMV secured frame format support (IEC 61850-90-5, IEC 62351-6)
- Cipher and decipher operation
- AES-GCM cipher suite
- Wire speed operation
- Minimum latency time for tightly real time constrained GOOSE and SMV messages
- Optimized FPGA resources utilization
- Combinable with SoC-e networking IPs

Secure Configuration-over-Ethernet IP

SoC-e developed a Layer 2 Ethernet based, configuration protocol to access to FPGA systems named Configuration-over-Ethernet (CoE). CoE is useful to access the FPGA from off-board CPUs or SCADA/PC systems using Ethernet data link. Secure Configuration-over-Ethernet IP is a new edition of this IP that supports secured CoE frames to allow the use of this protocol on open networks.

Key Features

- Configuration and control protocol over Ethernet between external CPU or SCADA/PC and the FPGA
- AES-GCM secured
- Optimized FPGA resources utilization
- Software API and program examples provided for the CPU or PC system

NIST800 Random-Number Generator IP

This IP implements a High Speed Random Number Generator (RNG) using FPGA resources. Random numbers form an integral part of most security systems. As an example, they are used is in the generation of cryptographic keys for data encryption. Also, RNG plays a vital role in the generation of the Initialization Vector (IV) for the secured communication frames.

Key Features

- High speed random sequence generation
- Minimum FPGA resources needed
- Device independent, no tuning required
- Circuit stabilized against jitter on the oscillator during operation
- NIST SP 800-22 and DIEHARD tests validated

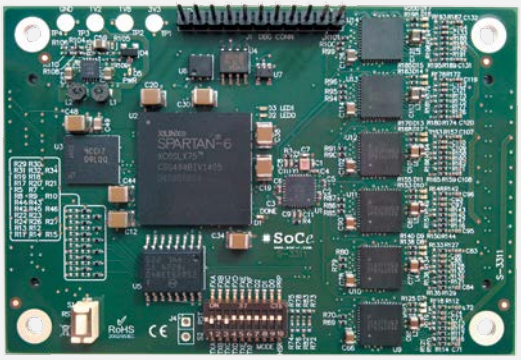
FPGA Networking Modules

SMARToem Family

SMARToem Family enables easy integration of added-value Ethernet Networks in equipment for Electric, Industrial and Aerospace sectors. The heart of the system is a Spartan-6 Xilinx FPGA able to drive up to 6 Fast Ethernet ports. The module can be used to implement a user defined design or can be purchased with any of the SoC-e Networking and Synchronization IP cores. This module is field proven worldwide embedding IEEE 1588-aware HSR/PRP and Ethernet switching capabilities into end-equipment like IEDs, relays, merging units and in distributed sensor infrastructures for traffic and transportation.

Applications

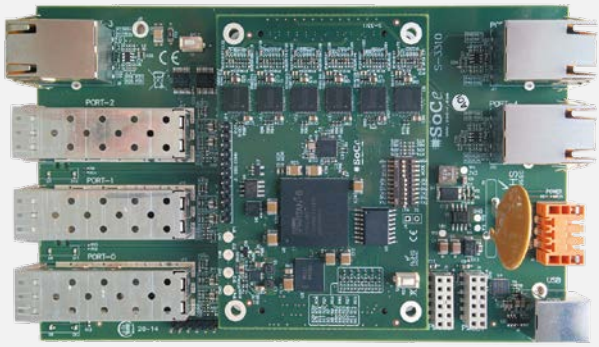
- HSR/PRP/Ethernet embedded switch
- IEEE 1588-2008 switch
- Custom Ethernet switch
- Industrial Ethernet Protocols gateways
- Cybersecurity applications
- Sensor Networks



Module

Key Features

- Scalable Spartan-6 Xilinx FPGA LX45-LX150
- Industrial Temperature Grade
- 6x Ethernet Phyters 10/100BaseT; 100BaseFX
- Support for Dynamic Bitstream Configuration (DBC)
- Support for Configuration-over-Ethernet (CoE)
- Optional 512 Mb LPDDR
- 128 Mb Quad SPI Flash: Memory for Firmware and bitstream storage
- EEPROM with unique MAC address
- Embedded Temperature Sensor



Brick

Key Features

- SMARToem module
- Carrier for SMARToem module
- 3x SFP cages for 100Base-X
- 3x RJ45 for 100Baset-T
- UART console (USB)
- 6V-30V DC (Power supply included)
- 2x PMOD connectors

FPGA Networking Modules

SMARTzynq Family

The heart of the SMARTzynq Family is a pluggable System-on-Module (SoM) designed to enable easy integration of specialized Gigabit Ethernet switches in smart equipment for Electric, Industrial and Aerospace sectors. The Zynq programmable SoC platform mounted in the board embeds a high-end FPGA and a dual core ARM9 CPU. This SoM is able to drive up to 5 tri-speed ports combining hardware IPs and software.

Applications:

- Managed HSR/PRP/Ethernet embedded switch
- IEEE 1588-2008 Master, Slave and Boundary Clock equipment
- TSN endpoint nodes and switches
- Smart gateways for heterogeneous networks interconnection
- Advanced Cybersecurity applications: NDIS, SIEM agents, on-the-fly encryption, etc.
- PCIe solution for SCADA and PC integration
- Out-of-the-box embedded CPU solution

Module

Key Features:

- Xilinx Zynq Programmable SoC XC7Z7020
- Industrial Temperature Grade
- Double core ARM9
- 5x Ethernet Phyters 10/100/1000BaseT-X; 100 BaseFX
- 8 Gb DDR3 RAM memory
- 256Mb QSPI Flash memory
- uSD card memory
- Size: 88x60mm

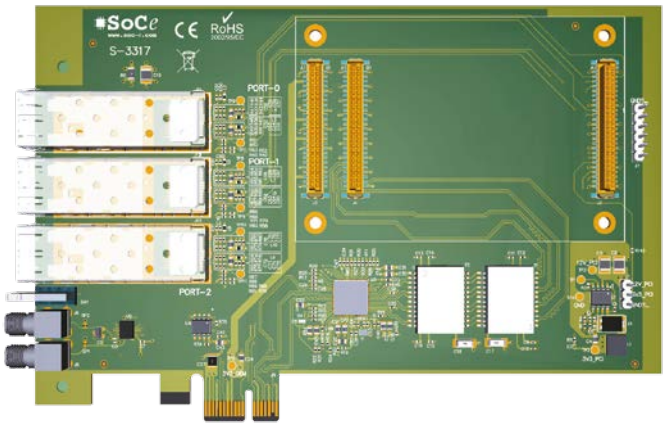
Brick

Key features

- 4x SFP cages for 10/100/1000BaseT-X; 100 BaseFX
- 1x RJ45 for 10/100/1000BaseT
- UART console (USB)
- 6V-30V DC (Power supply included)
- 2x PMOD connectors

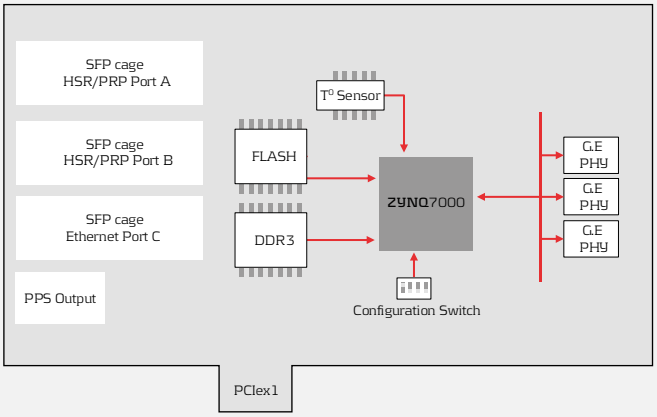
FPGA Networking Modules

SMARTzynq Family



PCIe

This PCIe solution enables a straight-forward integration of tri-speed HSR/PRP networks and IEEE 1588-2008 capabilities on SCADA and PC systems. The communication interfaces are tightly integrated with the Operating System of the host machine and the use of high availability networks is transparent for the software applications. The third network port allows additional REDBOX configuration that is managed autonomously by the PCIe card.



SMARTzynq PCIe can be used for many added-value applications apart from HSR/PRP. Synchronization platforms, as an example combining IEEE 1588-2008 and IRIG-B, can be implemented using this board. Also, SMARTzynq PCIe can host designs to access Industrial Networks, like Profinet, MRP or Ethernet IP. Additionally, added-value products for Cybersecurity based on this platform can be developed.

Key Features:

- 3x SFP cages for 10/100/1000BaseT-X; 100 BaseFX (copper and fiber optic)
- 2x SMA outputs for PPS, IRIG-B, etc.
- 1 PCIex1
- Software drivers: Windows distributions, Linux, VxWorks
- User-friendly configuration tool
- Middleware and API for Software developers
- Out-of-the-box configurations:
  - » HSR/PRP DAN (PC)+REDBOX
  - » 3x IEEE1588-aware Ethernet ports + PC port

Intelligent Gateways

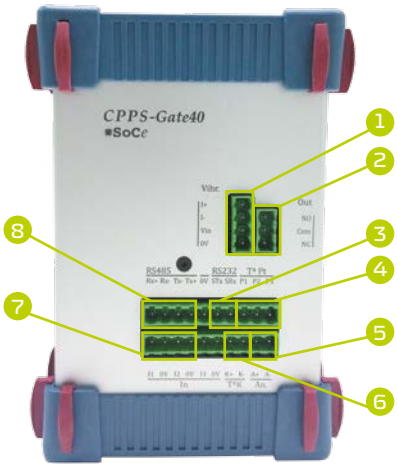


Fig. 1

CPPS-Gate40 Redbox

CPPS-Gate40 RedBox attaches Local Area Network (LAN) or conventional Ethernet equipment to zero-delay recovery time Redundant Ethernet networks. All this network switching operations are managed by hardware ensuring high data throughput and reliability. This Intelligent Gateway includes support for the latest IEEE1588-2008 version and profiles involved in the Substation Automation Systems enabling, as an example, the interconnection of IEEE1588-aware PRP networks with HSR ones.

Key Features

- HSR/PRP Support: IEC 62439-3 clauses 4 and 5, version 3
- Fiber optic or copper networking ports
- 4x SFP cages for 10/100/1000BaseT-X; 100 BaseFX
- 1x RJ45 for 10/100/1000BaseT
- Infrastructure for sub-microsecond synchronization: IEEE 1588-2008 OC, BC
- IEEE 1588-2008 profiles: Default, Power, Power-Utility, 802.1AS
- Multi-core CPU computation capacity for advanced managed operations like SIEM integration
- Cybersecurity add-ons at device level

CPPS-Gate40 Sensor

CPPS-Gate40 Sensor comprises in single equipment a flexible high-end networking switch, a powerful multi-core CPU and an integrated multi-sensor interface. These features combined with added-value hardware and software options enable cybersecure smart factory. This Intelligent Gateway merges the factory and the enterprise networks and provides means to pre-process data and to manage local and remote databases.

Key Features

- Multiprotocol support: Ethernet, HSR/PRP, Profinet, Ethernet IP, TSN, OPC UA, Modbus, Profibus
- Fiber optic or copper networking ports
- 4x SFP cages for 10/100/1000BaseT-X; 100 BaseFX
- 1x RJ45 for 10/100/1000BaseT
- Infrastructure for submicrosecond synchronization: IEEE 1588-2008 OC, BC and TC support
- Multi-core CPU computation capacity for big data and database processing
- Cybersecurity add-ons at device level
- Multisensor interface
- User customizable hardware and software design

Fig. 1

1. Accelerometer input
2. Potential-free relay output
3. Serial RS232 port
4. Temperature sensor input: Three-wire (PT100)
5. Analog input (current loop)
6. Temperature sensor input: Thermocouple Type K
7. 3x digital inputs
8. Half and full duplex RS485 port with Serial Modbus and Profibus support

Intelligent Gateways

VPX Gateway

SoC-e VPX processing unit, named SDRproc, is a 3U VPX VITA 48.2 REDI board. It embeds Texas Instruments OMAP processor (ARM9 + DSPC674X) and the powerful Xilinx Virtex-6 LX240 FPGA. This FPGA provides 5x 10 Gbps communication channels for VPX payload boards.

SDRproc is available for air cooled or conduction cooled operation and it is pluggable in Xilinx and Avnet development boards provided with FMC connectors using VPX2FMC adaptor.

Key features

- High-end Xilinx Virtex-6 FPGA
- Optional OMAP CPU module for flexible hardware/software processing partition
- Linux and Integrity G.H. BSPs
- 1Gb DDR3 and 512Mb Flash memory
- 20x Serial High Speed Channels-MGTs for data communication with payload boards
- Air-cool and conduction-cool versions for maximum guarantee in every condition

RSTP Posix-compliant Software Stack

SoC-e RSTPdstack is a portable C language, POSIX compatible, that implements RSTP processing according to the IEEE802.1D-2004 standard. The integration on Unix or VxWorks OS systems is straightforward. It can be used in combination with SoC-e MES IP or with other switches able to handle BDPU frames.

Key features:

- It implements IEEE 802.1D standard and processes all RSTP related events such as:
  - » Reception of a BPDU
  - » Identification of Physical Link status change
  - » Management of timeout 1 second
  - » Changes in the bridge parameters

As result of any of these events, the RSTP priority vectors and timing vectors are recalculated, and the following actions are performed:

- Transmission of BPDUs
- Switch's MAC table clearing
- Changes in switch's ports status

SoC-e Portable Tools

In order to simplify the integration and the use of SoC-e technology, we have developed a portfolio of portable software solutions. This portability allows implementations on SoC platforms, embedded CPUs or PC systems. The following list summarizes the software modules that integrate the SoC-e Portable Tools:

Key features

- Switch Management API
- SNMP Switch Management module
- WEB Switch Management module
- Network supervision module
- PTP software stack
- RSTP Linux stack
- MODBUS Server and Client stack
- PROFIBUS DP-Master stack

SoC*e*

System-on-Chip *engineering*

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If you are interested in knowing more about the solutions offered by SoC-e and their characteristics, we encourage you to contact us and tell us about your needs.
We will analyze your situation and use case scenario, and propose the standard or customized solution that best addresses your requirements.
Do not hesitate to request a quotation, or ask for any further information you require.